Exercises 1.12, 1.13, 1.14: Amplifier inputs/outputs

**1.12** A transducer characterized by a voltage of 1 V rms and a resistance of 1 MΩis available to drive

a 10Ωload. If connected directly, what voltage and power levels result at the load? If a unity-gain (i.e.,

) buffer amplifier with 1-Minput resistance and 10-output resistance is interposed between

source and load, what do the output voltage and power levels become? For the new arrangement, find

the voltage gain from source to load, and the power gain (both expressed in decibels).

**Ans.** 10 uV rms; 10­W; 0.25 V; 6.25 mW; 12 dB; 44 dB

**1.13** The output voltage of a voltage amplifier has been found to decrease by 20% when a load resistance

of 1 kis connected. What is the value of the amplifier output resistance?

**Ans.** 250 Ω

**1.14** An amplifier with a voltage gain of 40 dB, an input resistance of 10 k, and an output resistance

of 1 kis used to drive a 1-kload. What is the value of ? Find the value of the power gain in

decibels.

**Ans.** 100 V/V; 44 dB

Example 1.5: Freq response

Figure 1.25 shows a voltage amplifier having an input resistance Ri , an input capacitance Ci , a gain factor μ, and an output resistance Ro. The amplifier is fed with a voltage source Vs having a source resistance Rs, and a load of resistance RL is connected to the output.

(a) Derive an expression for the amplifier voltage gain as a function of frequency. From this find expressions for the dc gain and the 3-dB frequency.

(b) Calculate the values of the dc gain, the 3-dB frequency, and the frequency at which the gain becomes 0 dB (i.e., unity) for the case Rs = 20 kΩ, Ri = 100 kΩ, Ci = 60 pF, Ro = 200 Ω, and RL = 1 kΩ.

(c) Find vo(t) for each of the following inputs:

(i) vi = 0.1 sin 102 t, V

(ii) vi = 0.1 sin 105 t, V

(iii) vi = 0.1 sin 106 t, V

(iv) vi = 0.1 sin 108 t, V

Exercise 2.3: Op amp model

Example 2.1: Effects of finite gain; also include A=10^6

Example 2.2: “T” fdbk network

Exercise 2.6

Example 2.3: IA

**\*RD-1: For a real design problem, consider an available industry IA. Referring to the circuit**

**topology shown in the INA126 datasheet, analyze the circuit to verify the manufacturer’s gain**

**equation**

𝑮 = 𝟓 + 𝟖𝟎𝒌/𝑹𝑮

Section 2.5.2, “Miller Effect.” Also read, 9.4.4

Example 9.7: Miller effect

Read 10.2, “some properties of neg fdbk”

Section 2.6.2: note ib compensation methods

**\*RD-2: For modern op amps with ib on the order of pA, do you think explicit ib compensation—e.g.,**

**R3 in Fig 2.34, is necessary? Why or why not?**

Example 2.6: Closed loop freq response

Exercise 2.27: Freq response

Exercise 2.28: Freq response

Exercise 2.30: Full pwr bw

Chapter Problems

2.6 Common mode, differential mode signals

**\*2.9 Inverting Amp, resistor tolerance**

D2.2 Design an Inv Amp

2.25 Compensating for a finite A

**\*D2.42 Diff Amp design**

**\*2.43 IDAC; change to achieve 0** ≤**Vo** ≤**-3.3V**

D2.50 Analysis of Diff Amp using superposition

**\*D2.51 Var gain using pot**

2.53 Use of buffer

2.81 Miller effect

**\*D2.93 H(s) for op amp, Bode plot**

2.94 Eos

**\*2.95 Eos + signal**

2.107 Finite GBW

**\*D2.117 Cascading amps**

D2.118 More cascaded amps

2.125 SR

**\*D2.127 The compleat op amp designer**